



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,159	03/29/2004	Richard A. Blanchard	GS 124 D1	2962

27774 7590 11/08/2004

MAYER, FORTKORT & WILLIAMS, PC
251 NORTH AVENUE WEST
2ND FLOOR
WESTFIELD, NJ 07090

EXAMINER

NGUYEN, THINH T

ART UNIT	PAPER NUMBER
----------	--------------

2818

DATE MAILED: 11/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/812,159

Applicant(s)

BLANCHARD, RICHARD A.

Examiner

Thinh T Nguyen

Art Unit

2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 March 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 March 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED OFFICE ACTION

1. Claims 1-8 are pending in the Application.

Specification

2. The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant cooperation is requested in correcting any errors of which the applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102(b/e) that form the basis for the rejections under this section made in this office action.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 1,2 are rejected under 35 U.S.C. 102(b/e) as being anticipated by Williams (US patent 5,814,858) or Hsieh et al. (U.S. Patent 5,981,344) provided in the Applicant's IDS.

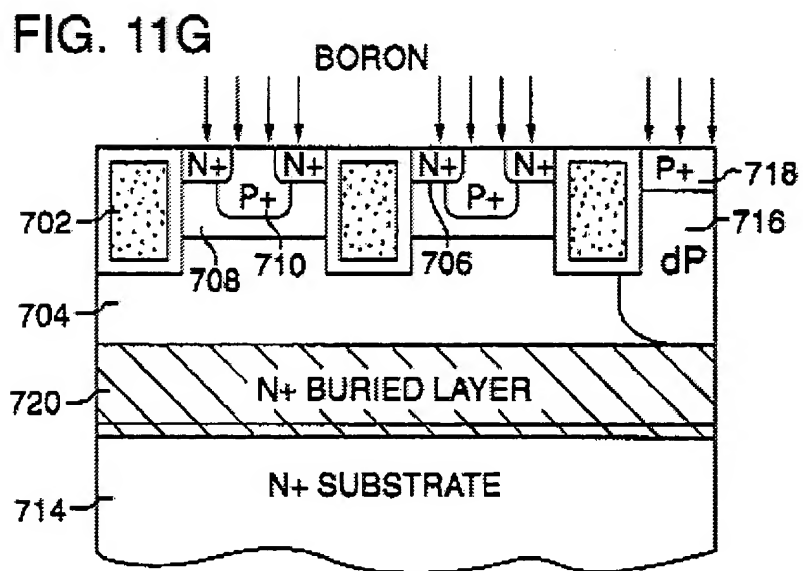
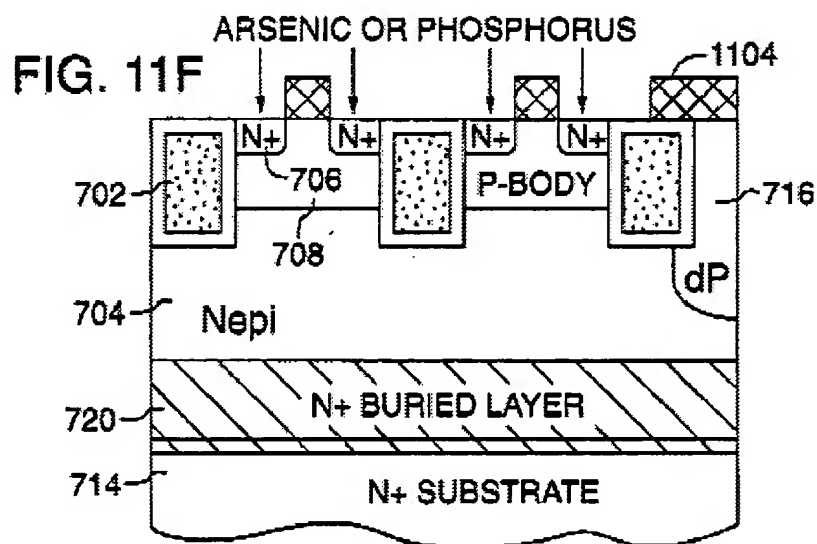
Art Unit: 2818

REGARDING CLAIM 1

Williams (the abstract, fig 11F, fig 11G, fig 5C, fig 5D) discloses a double diffused field effect transistor made in accordance with the method comprising: providing a substrate of a first conductivity type (fig 11G layer 714); introducing at least one dopant species of the first conductivity type into a surface of the substrate so that the substrate has a non-uniform doping profile; forming an epitaxial layer of the first conductivity type over the substrate (fig 11F layer 704), forming one or more body regions of a second conductivity type within the epitaxial layer; forming a plurality of source regions (fig 11F region 706) of the first conductivity type within the body regions; and forming a gate region (fig 11F region 702) adjacent to the one or more body regions.

Similarly, Hsieh et al. (the abstract, fig 4, layer 203, layer 202,layer 204,layer 206)

Disclose the same invention



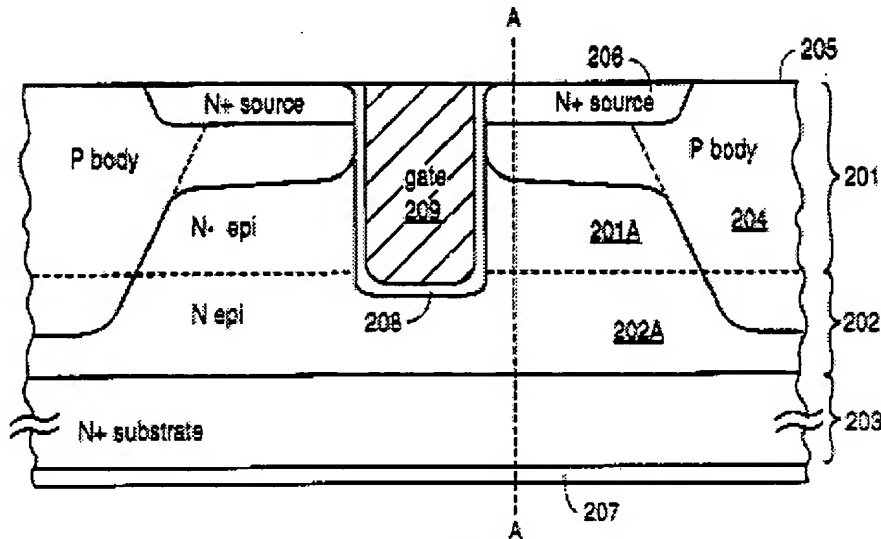


FIG. 4

REGARDING CLAIM 2

Williams (the abstract, fig 11D, fig 11F) discloses a double diffused field effect transistor made in accordance with the method wherein the step of forming the gate region includes the steps of: forming a plurality of trenches within the epitaxial layer; forming a first insulating layer that lines the trenches, and forming a polysilicon conductor within the trenches and overlying the first insulating layer.

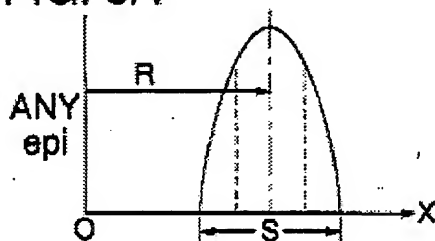
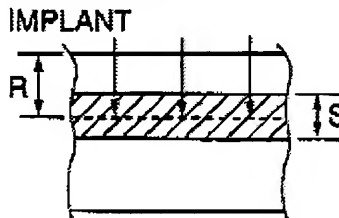
Similarly, Hsieh et al. (fig 4, column 1 line 57-58) disclose the same invention

5. Claims 3-6,8 are rejected under 35 U.S.C. 102(b/e) as being anticipated by Williams (US patent 5,814,858)

REGARDING CLAIM 3,4

Art Unit: 2818

Williams (the abstract, fig 5A, fig 5B, fig 11D, fig 11F) discloses a double diffused field effect transistor, comprising: a substrate of a first conductivity type; at least one dopant species of the first conductivity type incorporated into a surface of the substrate so that the substrate has a non-uniform doping profile, the non-uniform doping profile having a dopant concentration that is greatest at a given depth below a surface layer of the substrate and which decreases with increasing distance away from the given depth (fig 5A) ; and wherein said gate region includes a plurality of trenches located within said epitaxial layer; a first insulating layer (fig 11D layer 1102) that lines said trenches, and a polysilicon conductor (fig 11D layer 702) located within said trenches and overlying the first insulating layer.

FIG. 5A**FIG. 5B****REGARDING CLAIM 5**

The Examiner noted that claim 5 is a hybrid product by process claim for the recitation “ at least one dopant species is introduced into the substrate by ion implantation “.

In a product-by-process claim, it is the patentability of the claimed product and not of the recited process steps which must be established. Therefore, when the prior art discloses a product which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. The Patent Office is not equipped to manufacture products by a myriad of processes put before it and then obtain prior art product and make physical comparisons therewith. In re Brown, 173 USPQ 685 (CCPA 1972). Also, a product by process claim directed to the product per se, no matter how actually

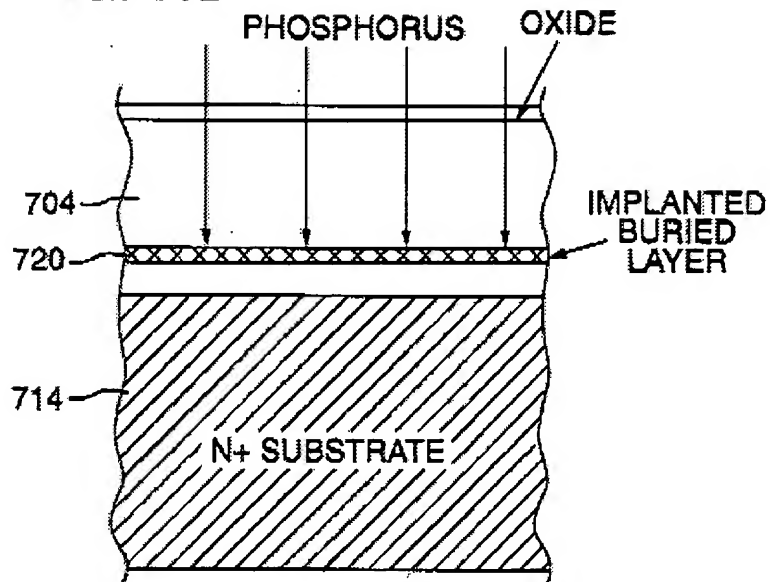
Art Unit: 2818

made, *In re Hirao*, 190 USPQ I S at 17 (footnote 3). See *In re Fessman*, 180 USPQ 324, 326 (CCPA 1974); *In re Marosi et al.*, 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process" claim, and not the patentability of the process. See also MPEP 2112.01 and MPEP 2113.

Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. Therefore, the limitation "introduced into the substrate by ion implantation" is not considered for the reason explained above.

Nevertheless, Williams does teach (fig 11B) that the impurities is introduced into the substrate by ion-implantation and therefore fully anticipated claim 5.

FIG. 11B

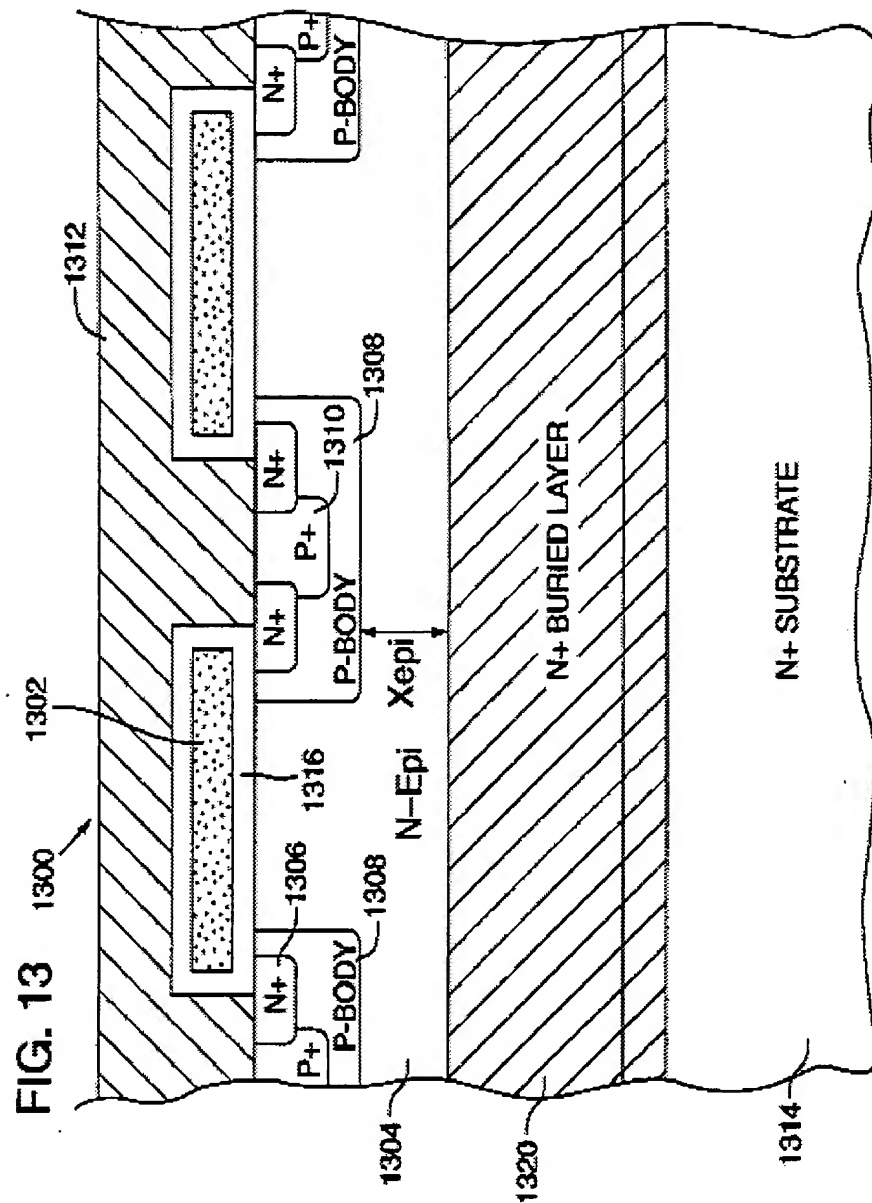


REGARDING CLAIM 6

Williams teaches (fig 11B) the use of phosphorus

REGARDING CLAIM 8

Williams discloses (fig 13) a double diffused field effect transistor comprising an electrode layer (fig 13 layer 1302) disposed on a surface of the substrate opposite the body regions.



Claim Rejections - 35 USC § 103

6. The following is a quotation of U.S.C. 103(a) which form the basis for all obviousness rejections set forth in this office action:

Art Unit: 2818

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Williams (U.S. patent 5,814,858) in view of further remark.

REGARDING CLAIM 7

Williams disclose all the invention except is silent about the use of an essentially uniform doping profile substrate. This feature, however, is considered obvious since the use of substrate with essentially uniform doping profile is old and well known in the art.

A person skilled in the art at the time the invention was made would have been able to include an essentially uniform doping substrate on the device invented by Williams without any special teachings as shown by Bulucea et al. (US patent 5,701,203), (column 10 lines 32-35) so that the device has good contact with the drain

8. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and the page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

9. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to be abandoned (see M.P.E.P. 710.02(b)).

CONCLUSION

10. The prior arts made of record and not relied upon are considered pertinent to applicant disclosure: Bulucea et al. (US patent 5,897,355) disclose a method of manufacturing insulated gate semiconductor device to improve ruggedness.


11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose telephone number is 571-272-1790.


The examiner can normally be reached on Monday-Friday 9:00am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached at 571-272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Thinh T. Nguyen 
Art Unit 2818


David Nelms
Supervisory Patent Examiner
Technology Center 2800